Leakage Control Techniques in Nanometer CMOS

The subthreshold leakage and gate leakage dominate the other leakage currents of the nanometer CMS. The latter is due to electrons tunnelling through the gate and onto the substrate. However, the former can be caused by a variety of factors. The leakage control techniques will therefore focus on subthresholds currents. Many techniques have been developed over the years to reduce subthresholds currents both in active and standby mode in order to minimize total power consumption in CMOS circuits.

Active leakage currents waste currents while the circuit in inactive mode, where no computation is taking place. In general, reducing leakage currents requires different circuit and device level techniques. On the device level it is possible to control the doping profiles of transistors and their physical dimensions, while on the circuit level it can be achieved by manipulating the threshold voltage (Vth), and the source biasing.

A. Circuit Level Leakage Control Techniques

i) Multi Vth Techniques

The technique involves the fabrication of high-Vth and low-Vth transistors on a single chip. The high Vth transistors are used to reduce the subthreshold current leakage, while the lower Vth transistors are used to improve performance by allowing faster operation. These different transistors can be obtained through channel doping controlled by the user, oxide thicknesses, channel lengths, or body biases. The implementation of high-Vth transistors will be a challenge due to the technology scaling and the continuous reduction in supply voltage.

Dual threshold method

This technique can be used to reduce leakage current in logic circuits by increasing Vth for devices on non-critical paths while maintaining performance at low Vth for critical paths. This technique can be used to control leakage power in both active and standby mode. This technique ensures the circuit runs at high speed with reduced power consumption.

Multi-Threshold Method

This method creates a virtual power supply by using a high-Vth device to gate the supply voltage of a low-Vth logic block. Instead of connecting the block directly to the main power, this method uses the high Vth to gate the voltage. High Vth switches are employed to disconnect power supplies in the standby mode, which results in extremely low leakage currents. In active mode, high Vth transistors will be switched on, and the logic blocks, which are designed with lowVth, will operate at a fast speed.

This allows for leakage current to be reduced via the high-Vth block and improved performance via the low-Vth block. This system can also be implemented by connecting a

high-Vth NMOS to the GND block and low-Vth block. The PMOS is not preferred over the NMOS because it has a higher ON-resistance and can therefore be made smaller. These transistors increase circuit delay and surface area. To retain data in standby mode an extra-high Vth memory is required.

Variable Vth Method

This method is used to reduce leakage currents in standby mode by adjusting the device dynamically by biasing the terminal of the body. By applying maximum reverse biasing in the standby mode Vth can be increased, and subthreshold currents are minimized. This method can also be used in active mode to optimize circuit performance. This tuning capability allows the circuit to operate with the minimum active leakage power.

Dynamic Vth Method

It is used to control leakage currents in circuits in active mode operation based on desired operating frequency. A back-gate bias is used to dynamically adjust the frequency in response workload. When the workload is low, increasing Vth will reduce the leakage power

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ii) Body Bias Control

By increasing the threshold voltages in MOS transistors, body biasing is an effective method to reduce both active and standby leakage. The Vth increases when the body bias is reversed. This reduces subthreshold current leakage. This can be achieved during standby mode, by

applying a negative bias to the NMOS and connecting the PMOS to the VDD rail. Body biasing can also be used to reduce DIBL and Vth-Rolloff that are associated with SCE. Body biasing is used in the Variable Threshold-CMOS technique. The Vth is directly related to the square root bias voltage, indicating that a high voltage would be required to increase the Vth. This could pose a challenge for the UDSM, where the supply is severely reduced.